REMARKS/ARGUMENTS

Claims 1-27 are pending in this application. Claims 1-27 stand rejected under 35 U.S.C. §112 as being indefinite. The Examiner objects to the language "direct circuit path". In order to improve the clarity of the claim, the word "direct" has been removed from the claim. Further, Applicants point out that the correction circuitry 160 of Fig. 4 is disposed in a circuit path between the power device 42 and the sensing circuitry including the comparator 46.

In view of the amendments, Applicants submit that the rejection under 35 U.S.C. §112 should be withdrawn.

The Examiner has also rejected claims 1-27 under 35 U.S.C. §102(b) as being anticipated by Masui, U.S. Patent No. 5,852,38. Applicants have amended the claims to recite that the correction circuitry included in the circuit path from the power device to the sensing circuitry for preventing the sense input signal on the circuit path from including spurious information received from the power device comprises an active impedance element for presenting a high impedance at the sense input when the power device is on, thereby allowing the spurious information to be conducted through the power device and presenting a low impedance at the sense input when the power device is off, thereby shunting said spurious information through said correction circuitry and preventing the sense signal from including the spurious information. With reference to Fig. 4, when the power transistor 42 is on, any spurious information, for example negative spikes on the DC bus, will be conducted through the power transistor 42. Under these circumstances, the comparator 164 senses the low level at the anode of diode 50 due to transistor 42 being on and maintains transistor 162 off thereby presenting a high impedance at the DS/VF input.

When transistor 42 is off, however, transients on the DC bus may be transmitted to the circuit by capacitive coupling through diode 60. The drain of transistor 42 is high when the transistor 42 is off, so diode 60 will be back biased. Transients on the DC bus can be transmitted to the circuit of Fig. 4 and can affect the sensing circuit 46 and the driver 44. In order to prevent this, the correction circuitry 160 and, in particular, the comparator 164 will sense that the DS/VF input is no longer low. As a result, comparator 164 will turn on FET 162 thus presenting a low impedance at the DS/VF input thereby providing an active impedance at the DS/VF pin and in

particular, a low impedance through FET 162 to sink a high frequency negative spike received as a result of capacitive coupling across the diode 60. See page 9, lines 15-25 of the specification.

Applicants have reviewed the Masui reference which relates to a power device driving circuit provided with an abnormality detecting circuit which detects the occurrence of an abnormality in the IGBT or a short circuit load based on a collector voltage of the IGBT which controls the gate voltage control circuit so as to gradually reduce the gate voltage of the IGBT. The IGBT is protected from breakdown caused by short circuit current increased by itself due to an inverse current from the load.

Applicants have reviewed the reference and it does not teach or suggest providing an active impedance at a sense input which changes depending upon whether the power device is on or off, thereby removing spurious information, for example, negative transient signals, from the sense input. Accordingly, Applicants submit that the invention as now claimed is not taught or suggested by the reference and accordingly, that all claims should now be allowed.

In view of the above, Applicants submit that all claims in this application are now in condition for allowance, prompt notification of which is requested.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 20, 2004:

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Signature

May 20, 2004
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Respectfully submitted,

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